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S P E C I F I C A T I O N

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TITLE: "PORTABLE BATTERY POWERED SYSTEM"

7/12/84

CROSS-REFERENCE TO RELATED APPLICATION

The present application is a continuation in part of my prior application U.S. Serial No. 385,830 filed June 7, 1982, now U.S. Pat. no. 4,455,523 and the disclosure and drawings of this prior application are incorporated herein by reference in their entirety.

BACKGROUND OF THE INVENTION

The present invention relates to portable battery powered systems and particularly to a battery system for portable devices capable of optimizing the performance of a rechargeable electrochemical storage medium while at the same time maximizing its useful life.

Portable computerized systems are presently being extensively utilized in a wide range of applications. For example, such systems may be utilized in delivery vehicles which are to be away from a central warehouse or the like for a major part of each working day. Recharging operations may take place in locations subject to extremes of temperature. It is particularly crucial to avoid an equipment failure where a portable device is a vital link to the completion of scheduled tasks at remote locations and the like. In such circumstances a loss of adequate battery power can be just as detrimental as any other malfunction.

SUMMARY OF THE INVENTION

05/25/84 612588 1 101 300.00 CK
05/25/84 612588 1 102 60.00 CK
05/25/84 612588 1 103 100.00 CK

It is a basic objective of the present invention to provide a portable battery powered system of increased reliability and useful life.

ISSUING TEXT P004

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An important feature of the invention resides in the provision of a portable system wherein the user can obtain a relatively accurate indication of the battery energy remaining available for use at any time during a portable operating cycle. Further, the user can be automatically alerted when battery capacity diminishes to a selected value, or when battery output voltage is at a selected marginal level.

For the sake of recharging of a battery system as rapidly as possible without detriment to an optimum useful life span, battery parameters including battery temperature can be monitored during a charging cycle and the battery charging current can be adjusted accordingly.

Since a battery may deteriorate when subjected to repeated shallow discharge and recharging cycles, according to the present invention, a count of such shallow charge cycles may be automatically maintained throughout the operating life of the battery system, such that deep discharge cycles may be effected as necessary to maintain desired performance standards.

Furthermore, according to another highly significant feature of the invention, automatically operating battery monitoring and/or conditioning circuitry may be secured with the battery pack for handling as a unit therewith. The monitoring circuitry may receive its operating power from the battery pack during storage or handling such that a total history of the battery pack may be retained for example in a volatile memory circuit where such type of memory otherwise provides optimum characteristics for a portable system. The conditioning circuitry may have means for effecting a deep discharge cycle, and concomitantly with the deep discharge cycle, a measure of actual battery capacity may be obtained. From such measured battery capacity and a continuous

measurement of battery current during portable operation, a relatively accurate "fuel gauge" function becomes feasible such that the risk of battery failure during field operation can be essentially eliminated. The performance of a given type of battery in actual use can be accurately judged since the battery system can itself maintain a count of accumulated hours of use, and other relevant parameters.

In a simplified system currently in use, the conditioning system is incorporated in the portable utilization device such that the programmed processor of the utilization device may itself automatically effect a deep discharge conditioning cycle and/or a deep discharge capacity test. The deep discharge cycle may be effected at a controlled rate, such that the time for discharge from a fully charged condition to a selected discharge condition may itself represent a measure of battery capacity. Instead of directly measuring battery current during use, the programmed processor may maintain a measure of operating time and/or elapsed time during portable operation, so as to provide an indication of remaining battery capacity.

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DRP The invention will now be described, by way of example and not by way of limitation, with reference to the accompanying sheets of drawings; and other objects, features and advantages of the invention will be apparent from this detailed disclosure and from the appended claims.

CL BRIEF DESCRIPTION OF THE DRAWINGS

P Fig. 1 is a somewhat diagrammatic perspective view of a portable battery powered device which may incorporate a battery system in accordance with the teachings and principles of the present invention;

P Fig. 2 is a somewhat diagrammatic enlarged longitudinal sectional view showing the battery compartment section and adjacent portions of the portable device of Fig. 1, with a battery pack assembly disposed in the battery compartment in operative coupling relationship with a central processing unit of the portable device for purposes of power supply to the central processing unit and for purposes of transmission of data and command signals;

P Fig. 3 is a somewhat diagrammatic perspective view of a battery system in accordance with the teachings and principles of the present invention;

P Fig. 4 is a perspective view similar to Fig. 3 but illustrating the battery system enclosed in a protective casing, to form a complete battery pack assembly for insertion into the battery compartment of the portable device, as a unit;

P Fig. 5 shows a block diagram for explaining the cooperative relationship of the electronic parts of the particular portable computer terminal device and battery system shown in Figs. 1 through 4, by way of example and not by way of limitation;

Fig. 6 ~~shows~~ a typical plot of permissible continuous overcharge rate as a function of temperature, for a particular type of rechargeable electrochemical energy storage cell, by way of example and not by way of limitation;

Fig. 7 ~~is~~ a plot of the effect of repetitive shallow cycling for the particular energy storage medium also represented by the plot of Fig. 6;

Fig. 8 ~~is~~ a plot of discharge characteristics for the particular energy storage medium also represented by the plots of Figs. 6 and7;

Figs. 9A and 9B ~~show~~ a specific circuit implementation in accordance with the block diagram of Fig. 5, by way of example and not by way of limitation;

Fig. 10 is a flow diagram for illustrating an exemplary control program for carrying out analog to digital conversion of battery parameter values utilizing the particular exemplary circuit of Figs. 9A and 9B;

Fig. 11 is a flow diagram illustrating the general battery processor control program utilized in conjunction with simplified system currently in use;

Fig. 12 is a block diagram of a simplified portable battery powered device in accordance with the present invention associated with a battery charger means, and also serves to illustrate a stationary battery conditioning system for spare battery packs;

Fig. 13 shows a specific implementation of the battery charge and deep discharge controller and monitor circuitry which is represented as a labeled rectangle in Fig. 12; and

Fig. 14 is a flow diagram indicating the operating means for effecting an automatic discharge cycle with the specific circuitry of FIG. 13.

DETAILED DESCRIPTION

Figure 1 is a perspective view of a portable battery powered device to which the present invention may be applied. The device is generally indicated by reference numeral 10 and is of a size to be conveniently held in one hand while a keyboard generally indicated at 11 is manually actuated by means of one or more fingers of the other hand. Characters entered by means of the keyboard 11 are displayed on a panel 12 under the control of a microprocessor located generally as indicated at 14 in Figure 2. At an end 15 of the portable device a battery receiving means or compartment is provided. Access to the battery compartment is obtained via a removable cover element 17. By unlatching and opening the cover element 17, a battery pack assembly such as indicated at 18 in Figure 4 may be inserted into or removed from the battery compartment.

By way of example, the battery pack assembly 18 may be comprised of rechargeable nickel-cadmium battery cells such as indicated at 21 and 22 in Figure 2. By way of example, four nickel-cadmium cells may supply a nominal output voltage of five volts and have a rated capacity of about 2.2 ampere-hours. By way of example, the central processing unit 14 of the portable device 10 may require an operating voltage of five volts plus or minus ten percent, so that a voltage regulator would be associated with the central processing unit so as to ensure an actual supply voltage within the range from 4.5 volts to 5.5 volts. The size and weight of the portable device together with the battery pack assembly 18 is such that the complete portable battery powered system can be held in one hand while the keyboard 11 is being operated with the fingers of the other hand.

In a typical use of the portable device 10, it is contemplated that the device may be used in an outdoor environment so as to be subject to a wide temperature range and relatively intensive daily use for example eight to ten hours per day. The battery pack assembly 18 is to be so designed as to have a maximum useful life even in such a stringent environment, thereby to ensure the maximum utility and reliability of the overall portable system as represented in Figure 1.

For the sake of ensuring optimum reliability and usefulness of the overall system of Figure 1, the battery pack assembly 18 includes digital processing circuitry 30 capable of data communication with the central processing unit 14 of the device 10. To this end, in the illustrated embodiment, as indicated in Figure 3, the battery means 20 including the rechargeable battery cells carries therewith a printed circuit board 31 having flexible electrically conductive straps 41 through 46 which automatically make firm and reliable electrical contact with connector strips such as indicated at 51 of the terminal device 10. Two of the conductive straps of the set 41-46 may be connected with the opposite polarity terminals of the 14 battery means 20 so as to supply battery voltage to the regulator means of the central processing unit 14. The remaining straps of the set 41-46 may serve to provide a communication channel between a 14 battery processor unit of the processor circuitry 30 and the central processor unit 14 of the terminal device 10.

Referring to Figure 4, the battery pack assembly 18 may include an insulating casing part 60 which has an aperture at 60a in Figure 4 for exposing the conductor straps 41 through 46 for resilient pressure engagement with respective cooperating terminal connectors such as indicated at 51 in Figure 2. As

indicated in Figure 2, the dimensions of the battery compartment of the device 10 are closely matched to the dimensions of the battery pack assembly 18 so that the battery pack assembly 18 can only be fitted within the battery compartment in such a way that the straps 41 through 46 are in firm engagement with the respective terminal connectors such as 51.

From Figures 2, 3 and 4, it will be understood that the processor circuitry 30 including the conductive straps 41-46 is secured with the battery means 20 for removability from the battery compartment as a unit. Thus the battery pack assembly 18 has self-contained processor circuitry as indicated at 30. As will be explained hereinafter, this processor circuitry 30 is electrically coupled with the battery means 20 so as to receive operating power therefrom both while the battery means forms part of the portable system 10 and while the battery means is separate from the portable unit. Thus, even where the processor circuitry 30 is provided with a memory requiring a constant supply of power, data is not lost from the memory upon removal of the battery means from the portable device 10. Still further as will be hereinafter explained the processor circuitry 30 including its memory may be operable with a battery voltage substantially less than that required by the central processor unit 14, so that data is not lost from the memory of the processing circuitry of the battery pack assembly even where the battery means has been discharged so as to have a relatively low output voltage below the minimum required operating voltage for the central processing unit 14. In this way, the battery memory means is enabled to retain an operating history of a particular rechargeable battery pack over the entire life of such battery pack, while on the other hand the processor circuitry 30 is designed so as to require a minimum space

beyond the outline configuration of the rechargeable battery cells themselves. In Figure 2, it will be observed that the casing 60 is relatively closely spaced to the periphery of the battery cells such as 21 and 22 in comparison to the cross sectional dimensions of such battery cells, and that the processor circuitry 30 is of a width dimension as viewed in Figure 2 so as to at least partially fit within a nitch such as indicated at 63 between the two sets of battery cells. Still further, such processor circuitry 30 is selected so as to provide an essentially minimal power drain on the battery means 20, such that the battery means may be stored for long periods of time without loss of the data stored in the battery memory means. For example, the processor circuitry 30 including its associated memory means may require only a few percent of the current required by the processing system of the portable unit 10. For example, a shelf life of from one to two months for the battery memory means is feasible.

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CL/1 Description of Figure 5

P Figure 5 illustrates an overall exemplary circuit diagram for the embodiment of Figures 1 through 4. In Figure 5, reference numeral 71 indicates a terminal processor component including central processing unit 14 and associated memory circuits. Component 72 in Figure 5 represents terminal display circuits which may be associated with the display screen 12 of Figure 1. Terminal connectors such as 51 are also diagrammatically indicated and are shown as being electrically connected with the flexible straps 41 through 46, respectively, of the battery pack assembly.

In Figure 5, the battery pack or rechargeable battery means is again generally designated by reference numeral 20, and the positive and negative output terminals of the battery means 20 are indicated as being connected with the terminal processor and memory circuits component 71 via electrically conductive straps 45 and 46.

Reference numeral 81 in Figure 5 designates a digital interface component which serves for the coupling of the terminal processor of component 71 with a battery processor of component 82 of the battery pack assembly 18. Simply for the sake of example, communication between the battery processor of component 82 and the terminal processor of component 71 is indicated as taking place via three conductors which include respective conductive straps 41 through 43 of the battery pack assembly 18, Figure 4. Further details of an exemplary digital interface circuit for implementing component 81 will be given in relation to a more detailed electric circuit diagram to be described hereinafter. For the sake of correlation with the

detailed circuit to be later described, reference numeral 83 designates a voltage regulator and reset circuit. Component 83 serves to supply a regulated operating voltage to the component 82 as well as to circuits of the digital interface component 81 in a specific preferred implementation of the present invention to be described hereinafter. Component 82 in such specific example includes a memory which requires a continuous operating voltage in order to maintain a continuous history of the battery means 20. The reset circuitry of component 83 is a dapted to supply a $\overline{\text{RESET}}$ signal which serves to indicate that the memory means has had its operating voltage interrupted.

Components 91, 92 and 93 in Figure 5 represent battery monitoring means operatively coupled with the battery means 20 for the purpose of obtaining quantitative measures of respective battery parameters. Where the respective parameter sensing means of components 91, 92 and 93 supply analog signals, digital to analog converter means may be associated with the monitor circuitry for the purpose of obtaining the quantitative parameter measurements in digital form. In a particular preferred arrangement to be hereafter described in detail, the battery processor of component 82 may supply digital reference signals via the line 95, and the digital reference value may be converted into a common analog reference signal for matching with the respective analog measurement values of components 91, 92 and 93. In this particular embodiment, comparator circuits may be included in components 91, 92 and 93 for comparing the respective analog measurement signals with the common analog reference value in a predetermined order, the logical output signals from the comparator means being supplied via lines 96, 96 and 98 to the processor means for signaling when the digitally generated analog reference signal has reached a level exceeding the analog

measurement value being compared therewith. The digital measurement values so determined may be utilized as a basis for updating battery condition information in the memory of component 82.

A battery charging voltage input is indicated by the
30 symbol "+CHG". Battery charging current is supplied to the rechargeable battery means 20 via a battery charging current path which is controlled by a battery charging controller circuit 101 which may receive a digital battery charge control signal via line 102 in Figure 5. According to a preferred embodiment to be described in detail hereafter, the battery charging current path further includes a battery current sensing means which forms part of component 92. The arrangement is preferably such that the battery current measured by component 92 during a charging operation does not include any charging current which may be supplied to the terminal device including components 71 and 72 in Figure 5. Thus the battery processor of component 82 during a charging operation receives from component 92 a quantitative measure of actual charging current supplied to the battery means itself. A battery charging voltage monitor 103 is operatively coupled with the battery
30 charging voltage input "+CHG" and is operative to supply a quantitative measure of battery charging voltage to the processor circuitry of component 82. For example, in a preferred arrangement, the digital reference value supplied by line 95 in Figure 5 is utilized periodically to generate an analog reference value for comparison with the analog reading of battery charging voltage of component 103. In this case, a comparator circuit of component 103 signals via output line 104 when the analog reference value exceeds the currently occurring analog

value of the battery charging voltage. Thus, during a battery charging cycle, the battery processor of component 82 is supplied with battery operating information from which an optimum battery charging current can be selected. In particular, by sensing battery temperature during the battery charging operation, it is possible to provide a battery system which is adaptable to operation under a wide range of environmental conditions while yet assuring optimum efficiency in carrying out a battery recharging operation.

For further assuring the optimum conditioning and maximum operating life of the battery system, Figure 5 illustrates a battery deep discharge controller component 110 as being electrically connected with the battery means and being controlled by an input line 111 for effecting a deep discharge conditioning of the battery means 20 at suitable times during the operating life of the battery means. In accordance with the teachings of the present invention, during the deep discharge cycle of the battery means, battery current is continuously measured by the battery current monitoring component 92 so as to enable the battery processor and memory circuits of component 82 to derive a quantitative measure of the available capacity of the battery means. In a relatively simple determination of battery capacity, the battery means 20 may be first fully charged, and then subject to a deep discharge cycle wherein the battery means is discharged at a predetermined rate until such time as the battery means 20 exhibits a battery output voltage of a predetermined value, for example, four volts where components 71 and 72 of the terminal device require a minimum operating voltage of say 4.5 volts. By way of example if the battery means

has a nominal rated capacity of 2.2 amp hours, the battery may be discharged at a rate of 220 milliamperes (battery capacity C divided by ten). In this case a deep discharge cycle would be completed within not more than about ten to twelve hours. (See Figure 8 which represents the discharge characteristic of one nickel-cadmium cell.)

Charge current is coupled to the battery pack via conductive strap 44 of Figure 5.

CL 4/1 Description of Figures 6 and 7

P By way of background, Figure 6 is a plot illustrating maximum charge rate as a function of temperature. It will be observed that at relatively low temperatures, the permissible charging rate is relatively low. Thus a battery system adaptable to a wide range of environmental conditions, and yet utilizing a maximum charging rate is achieved when the charging rate can be adjusted according to quantitative measurement of battery temperature during the charging cycle.

Specifically for the case of a nickel-cadmium battery pack overcharging is the point at which the majority of charge current generates oxygen at the positive electrode rather than increasing the state of charge of the cell. This point occurs at approximately the 75% state of charge level. As oxygen is generated, the internal pressure of the cell increases, which ultimately determines the amount of overcharge the cell can withstand. The maximum allowable rate is a strong function of cell temperature. This is due to the fact that the generated oxygen must re-combine with cadmium at the negative electrode to prevent oxygen build-up and hence internal pressure increase. The rate of re-combination is dictated by cell temperature due to the viscosity of the electrolyte and the rate of the chemical reaction at the negative electrode. If the allowable over-charge rate for a given cell temperature is exceeded, the cell pressure may exceed the pressure relief valve safety level, causing venting and potentially expelling electrolyte, which drastically reduces cell life.

Figure 7 illustrates the effect of repetitive shallow cycling on the output voltage of a given cell of a nickel-cadmium battery pack. Curves 121, 122 and 123 show the variation in output voltage over an operating cycle for respective increasing numbers of shallow operating cycles. Specifically curve 121 shows the variation in output voltage over time in hours for shallow discharge cycle number 5, while curve 122 represents the corresponding variation at shallow cycle number 100 and curve 123 shows the result at cycle number 500. Not only does repetitive shallow discharge produce a voltage depression effect as illustrated in Figure 7, but this type of operation of the battery pack also causes a gradual and consistent degradation of cell capacity.

CL½ Description of Figure 8

P Figure 8 illustrates the discharge characteristic for a nickel-cadmium cell. A deep discharge of the cell is considered to have taken place at region 124 where the output voltage begins to decrease relatively rapidly. A deep discharge cycle may be considered to have been effected when the cell voltage falls to a value of one volt, for example. A deep discharge, at a normal rate of battery usage, say battery capacity divided by twenty (C/20), might require more than twenty hours of portable operation without a recharging cycle.

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Description of Figures 9A and 9B

Figures 9A and 9B illustrate a more detailed circuit implementation in accordance with the block diagram of Figure 5. In Figure 9A the battery pack is schematically indicated at 20 and is shown as having a precision resistance element 131 permanently in series therewith for the purpose of sensing battery current during charging and discharging operations. By way of example, element 131 may have a resistance value of one-tenth ohm with a precision of one percent. The battery pack 20 also has associated therewith a precision voltage sensing arrangement comprising resistance elements 132 and 133. The resistance value of elements 132 and 133 in series is sufficiently high so that only a negligible battery current flows in this voltage sensing circuit. A battery temperature sensing transducer 134 is shown as being physically disposed in heat transfer relation to the battery pack 20. A precision resistance element 135 is shown in series with the transducer 134 for the purpose of supplying a voltage representative of battery temperature during a charging operation.

For the purpose of sensing charging voltage during a battery charging operation, precision resistance elements 136 and 137 are illustrated as being connected with the battery charging voltage input "+CHG". The resistance values of the voltage divider are selected such that the voltage across resistance element 137 will accurately represent the charging voltage during a battery charging operation.

Analog to digital converter means is associated with the respective battery parameter sensing elements so as to convert the measurements into digital form. In the particular circuit embodiment illustrated in Figures 9A and 9B, this conversion operation is carried out with the use of programmed processor circuitry 140, Figure 9B. The processor circuitry 140 controls an eight-bit R/2R ladder network 141 having an analog output at 142. The analog output line 142 is connected to comparators 151 through 154 shown in Figure 9A and supplies a common analog reference voltage to the non-inverting inputs of these comparators. The inverting inputs 161 through 164 of the comparators 151 through 154 are coupled with the respective battery parameter sensing circuits. In a specific implementation, the processing circuitry 140 is implemented with a power supply voltage of three volts which may be obtained from a very accurate stable voltage reference supply/amplifier device 150. By utilizing a voltage reference as the power source for the processing circuitry 140, the output ports associated with the ladder network provide an accuracy comparable to that of a conventional digital to analog converter. In the particular embodiment illustrated there is a ninth bit in the most-significant bit location of the ladder network 141. This is provided so as to adapt the ladder network output at 142 to the input common mode voltage range of the comparators 151 through 154. Under worst case conditions, the battery terminal voltage may reach 4.0 volts which limits the common mode input voltage to 2.5 volts, approximately. To achieve eight-bit resolution, the full digital to analog analog voltage range must be accommodated by the comparators 151 through 154. By configuring the digital to

analog converter network 141 as a nine-bit ladder with the most significant bit a logic zero, the lower eight bits of the nine-bit ladder remain, giving a resultant digital to analog voltage range of:

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$$0V. \leq D/A\ output \leq \frac{255}{511} Vref. \quad (=1.497V)$$

$$V_{step} = \frac{Vref.}{511} = 5.87mv/step,\ 256\ steps$$

PS so: digital output 0 = 0 volts
digital output 255 = 1.497 volts

P With this digital to analog converter as a building block, a successive approximation analog to digital converter can be implemented with the voltage comparators 151 through 154 Figure 9A and a straightforward microprocessor algorithm (as represented in Figure 10).

The successive approximation algorithm depends on the assumption that the analog voltage being measured does not change appreciably during the conversion sequence. The nature of the exemplary application inherently has characteristics of slowly changing parameters with the exception of the discharge current, which can change abruptly and significantly. The solution to this potential difficulty is a low-pass filter amplifier which serves to integrate or average any rapidly changing current fluctuations.

Since the analog to digital converter has a conversion range of 0 to 1.497 volts, the four analog signals to be measured must be scaled appropriately to yield a convenient step resolution by offering measurability over the necessary range of values. The scaling values and step resolutions may

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be selected as follows:

1. Channel 0: Charge voltage
   - step resolution = 80mv
   - maximum range: 20.40 volts
2. Channel 1: Discharge current
   - step resolution = 2ma
   - maximum range: 510ma
3. Channel 2: Battery terminal voltage
   - step resolution = 25mv
   - maximum range: 6.375 volts
4. Channel 3: Battery temperature
   - step resolution = $2^{o}K$
   - maximum range: $509K = 236^{o}C$

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Particularly in the case of channel two it might be noted that a four-cell nickel-cadmium battery pack can have a terminal voltage that exceeds 6.375 volts, which is the maximum range of channel two. In the present example, however, no additional useful information would be provided if the battery processor could determine when battery voltage exceeded 6.375 volts.

As previously mentioned, battery discharge current is subject to rapid fluctuations. Accordingly, the channel one current monitor means includes an integration circuit as indicated at 170 in Figure 9A. The integration circuit 170 has its input connected with the current sensing resistance element 131 and its output connected with input line 163 of comparator 153, Figure 9A.

Referring to Figure 9A, an implementation of the battery charging controller 101 of Figure 5 comprises an analog control line 171 leading to an inverting input of a comparator 172 which controls a battery charging current regulating circuit 173. The battery charging current is controlled by the processor circuitry 140, Figure 9B, with the use of an additional four bit R/2R ladder network 174. The ladder network 174 supplies an analog command signal via line 171 for controlling components 172 and 173. Thus, the analog command signal can have one of sixteen discrete voltage levels. The output voltage range is from zero volts to 15/16 times the reference voltage level or 2.81 volts, with steps of 187.5 millivolts.

An operational amplifier 176, Figure 9A, is coupled with the battery current sensing resistor 131 and provides an amplification such that a voltage step of 187.5 millivolts at input 171 of comparator 172, Figure 9A, is matched by a battery current step of thirty-two milliamperes in resistance element 131. Thus, for a battery current in element 131 of thirty-two milliamperes, a voltage at output line 177 of 187.5 millivolts is supplied to the non-inverting input of comparator 172. The minimum charge current level is theoretically zero; however, finite input offset voltages present in the amplifier 176 predict a potential zero level charge current of six milliamperes maximum. This is insignificant when it is recognized that the only time the zero level charge value will be selected is during the deep cycle function when much larger current levels will be drained from the battery.

In the illustrated battery charging current regulating circuit 173, three power transistors in parallel have separate base resistors for balancing unequal device parameters and ensuring equal current and power dissipation sharing between the devices. A major design consideration in the illustrated embodiment is the power dissipation of the current regulator 173 coupled with the heat associated with the battery pack 20 during the charging cycle, especially during the overcharge portion of the charge cycle which occurs after the battery reaches approximately seventy-five percent of its maximum charge capacity. To retain compatibility with existing charging circuits, the regulated charger 172, 173 must be capable of operating with input charge voltage levels of at least twelve volts. In some instances, the applied charge voltage might exceed eighteen volts. The dissipation is the regulator devices of circuit 173 is given by the equation: PS

T1 $$P_d = (V_{CHG} - V_{BATT})\ I_{CHG}$$

PS Given worst case conditions: $V_{CHG} = 18$ volts
$V_{BATT} = 4$ volts
$I_{CHG} = 480$ ma PS

T1 $$P_d = (18-4)(.48) = 6.72 \text{ watts}$$

P It is clear that 6.72 watts exceeds the power dissipation capacity of even three transistors in regulator network 173, and would generate excessive heat within an enclosed unit even if the transistors could handle the charge voltage input. Since the battery voltage is known and the charge current level is selected by the processor circuitry 140, the resultant power dissipation can be directly controlled by the processor circuit 140. This means that essentially constant power operation of

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the transistors of network 173 can be achieved when high charge voltage conditions exist. If the charge voltage input is reduced to a more efficient level, higher charge currents are possible when conditions permit. The minimum charge voltage input that would still give proper constant current regulation is approximately 7.0 volts, which would result in minimum power dissipation.

According to the teachings of the present invention, the battery pack 20 is to be subjected periodically to a deep discharge cycle, in order that the battery pack can maintain its full rated capacity and exhibit maximum operating life. A suggested discharge cycle to meet this requirement is discharging the battery at a C/10 rate to a terminal voltage of 4.0 volts for a four-cell configuration. A discharge control circuit for this purpose is indicated at 180 in Fig. 9A, the control input 181 being controlled from the processor circuitry 140 as indicated in Fig. 9B.

A deep discharge of battery pack 20 would not normally occur in the typical usage contemplated for the illustrated embodiment since normally the battery pack and associated portable system is used less than fourteen hours per day, while the design operating time for the battery pack is typically twenty hours. Furthermore, most logic devices and LSI circuits such as those utilized to implement component 71 of Fig. 5, will not function at 4.0 volts. The illustrated embodiment performs the deep discharge function by switching a resistive load 182, Fig. 9A, across the battery 20 that causes current to be drained out at a predetermined rate, typically C/10. During the deep discharge cycle, not only is the battery conditioned, but further, according to the teachings of the present invention, the available capacity of the battery is

measured. By measuring the available capacity of the battery, a battery "life history" can be maintained that has important diagnostic potential. If the available capacity begins to decrease past predetermined values, the user can be alerted, for example, via the terminal display circuits component 72, Fig. 5, before a fault or field failure occurs. The battery current sensor element 131 and integrator circuit 170 may be utilized to measure battery capacity during the deep discharge cycle.

In order to allow the battery to be discharged down to a deep discharge level corresponding to an output voltage of 4.0 volts, an auxilliary power source should be available to power the logic in the portable terminal device of Fig. 5 during the deep discharge cycle. A power regulator circuit may be built into the portable terminal device that regulates 5.0 volts from either the battery 20 or the charge voltage input terminal "+CHG", whichever is higher in potential. The net result of this power control arrangement is to completely remove the terminal load from the battery whenever the system receives power from a charger. For the case of a portable terminal device having data in a volatile memory, it is necessary that the charge voltage input not be interrupted during a deep cycle sequence. A message at the display 12, Fig. 1, can inform the user that the deep cycle sequence is in progress and that the terminal device should not be used until the cycle is completed. To minimize the impact of this operation on the user, the deep cycle function including a full discharge followed by a normal charge cycle will be initiated by the application program in the terminal device so that a convenient non-interferring time can be selected for this relatively long duration function, for example, over a weekend.

The key to utilizing the functional capabilities of the battery processor 140 is to provide for digital communication between the battery processor and the terminal processor circuitry. A digital interface 81 has been indicated in Fig. 5 for this purpose and exemplary detailed circuitry in Fig. 9B has been given the same reference numeral. The interface 81 may process the following three data signals:

1. BPCLK: Battery Processor Clock (from terminal)
2. BPWDATA: Battery Processor Write Data (from terminal)
3. BPRDATA: Battery Processor Read Data (from battery processor)

These three signals are protected from damage by static discharge by means of one hundred kilohm resistors in line with each input or output. The battery processor interface utilizes voltage comparators 191, 192 and 193 which are relatively immune to static damage. At the terminal, CMOS devices are used, therefore 4.7 volts Zener diodes are provided to further protect these more sensitive components. The voltage comparators 191, 192 and 193 perform the additional function of level conversion between the battery processor operating at 3.0 volts and the terminal logic operating at 5.0 volts. The open collector outputs of the comparators are pulled up by resistors connected to the appropriate power supply to ensure proper logic levels in either direction.

The communication protocol is based on the terminal processor controlling data transfers by issuing a clocking signal to the battery processor. The battery processor has the capability of requesting service by causing an interrupt to the terminal processor when it pulls the BPRDATA signal from its rest "1" condition to a "0". This signal has a resistor pull down on the terminal side of the interface, so an interrupt will automatically occur whenever the battery pack is removed from the terminal.

It is recognized that complete discharge of the battery can occur. In this case, information stored in the battery processor circuitry 140 will be lost but the system must be able to restore itself and properly recover and recharge the battery. To ensure such recovery, a voltage comparator 195 monitors the 3.0 volt power supply 150 and forces a $\overline{\text{RESET}}$ condition if the voltage supplied to the processor goes out of range. When the battery pack is again placed on charge, the battery processor circuitry 140 will restart and the control program will re-establish execution and control of the battery system.

Where the battery pack assembly 18 could be accidentally inserted upside-down, and reverse the electrical connections, to prevent damage or operational faults, the interface signals are shown as being arranged so that no high powered signals are connected to other high powered signals if reversed. All reversed connections terminate through the 100 kilohm protection resistors at the strap conductors 41-44, limiting currents to safe levels.

By way of example, processor circuitry 140 may be implemented by means of a single chip microprocessor such as the MC146805F2 which is a high performance CMOS derivative of the MC6805, with a reduced pinout arrangement that allows packaging in the JEDEC standard twenty-eight pin leadless chip carrier. Features of this device include:

1. Operation at $V_{CC} = 3.0V$
2. Low power standby "sleep" mode with self wake-up
3. External interrupt
4. Miniature package
5. CMOS port structure
6. On chip clock oscillator

By way of example, a one megahertz crystal is indicated at 196 in association with the clock oscillator terminals of circuitry 140.

CL 1/(Description of Figure 10

Figure 10 illustrates a successive approximation algorithm for carrying out analog to digital conversion with respect to one of the battery parameters sensed by the circuitry of Figure 9A.

By way of specific example, if a battery charging operation is to take place and if the charge voltage at "+CHG" is 14.385 volts, then the voltage at input 164 of comparator 154 will have a value of 1.050 volts. Thus, at the start of a conversion operation for obtaining a digital measurement of charge voltage, as represented at 10-1 in Figure 10, the analog voltage at the reference input line 142 will be at zero volts, and the output of comparator 154, designated AN0 (channel 0) will be at a logical zero level.

As represented at block 10-2 in Figure 10, for the case of an eight-bit digital to analog converter network 141 as previously described, a variable n is initially assigned a value seven. According to step 10-3, a logical one value is thus assigned to the highest order output port of processor 140. The result is that the reference line 142 receives an analog output voltage corresponding to 2^7 or 128 voltage increments (about 0.751 volts). Since the analog reference value at line 142, Figure 9A, is still less than the analog voltage at line 164, comparator 154 continues to supply a logical zero signal to the processor 140.

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According to the block 10-4 of Figure 10, the comparator output logic level is read by the processor, and according to decision block 10-5 where the comparator output is at a logical zero, processing continues via block 10-6 to block 10-7, whereby the variable n is assigned the new value six.

Thereupon, upon return to step 10-3, a logical one signal is produced at the second highest order output port of processor circuit 140, so that a total of 192 voltage increments is supplied at analog reference line 142 (a voltage of about 1.127 volts). If the voltage level at line 164, Figure 9A, is 1.050 volts, then the voltage level at line 142 now exceeds the voltage level at line 164, and the output of comparator 154 is at a logical one level. Accordingly at the decision step 10-5, the program branches to block 10-8, whereby the bit with the weight of 2^6 is set to a logical zero value. Then according to step 10-6 and step 10-7, the variable n is set to five, and according to step 10-3 the bit with the weight of 2^5 is set to a logical one value. Accordingly, analog reference line 142 receives a voltage of 160 voltage units (0.939 volts). Since the analog reference level at line 142 is now less than the analog value at line 164, comparator 154 supplies a logical zero signal, and processing continues through steps 10-4, 10-5 and 10-6. Next according to step 10-7, the variable n is set to a value of four, and so on. When finally the bit having a weight of 2^0 has been set by the procedure of Figure 10, the program branches to 10-9, and the analog input value at 164, Figure 9A, has been converted into a corresponding digital value which may be stored in the memory of component 140 for further processing.

CL ½

Description of Tables A and B

On the following pages a Table A and a Table B pertaining to the battery processor component 82, Fig. 5, are set forth. In Table A, various suggested hexadecimal (HEX) codes are set forth which may be utilized in conjunction with the keyboard 11 (Fig. 1), for transmitting commands to the battery processor. In the case of hexadecimal codes 30 (HEX) through 35 (HEX), the requested battery information is transmitted by the battery processor via the digital interface 81, Fig. 5, for display on the terminal display screen 12, Fig. 1.

Table B illustrates the type of data which may be stored at respective memory locations of the memory circuits of component 82, Fig. 5. While the Tables are considered self-explanatory, a few comments on Table B are presented subsequent to the Tables:

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T0330X

TABLE A

BATTERY PROCESSOR: COMMAND FORMAT

CODE (HEX)	FUNCTION
00	Error recovery RESET
01	Read STATUS (one byte returned)
02	RESET ALL, Begin history
10	Read analog channel 0 (one byte returned)
11	Read analog channel 1 (one byte returned)
12	Read analog channel 2 (one byte returned)
13	Read analog channel 3 (one byte returned)
20	Set low reserve alert point (one byte sent)
21	Set low voltage alert point (one byte sent)
22	Set minimum capacity alert (one byte sent)
30	Read fuel gauge (one byte returned)
31	Read maximum available capacity (one byte returned)
32	Read charge cycle count (two bytes returned)
33	Read deep cycle count (two bytes returned)
34	Read accumulated hours used (two bytes returned)
35	Read use history indicator (four bytes returned)
40	Initiate deep cycle function

33

T0340X

TABLE B

BATTERY PROCESSOR: DATA DEFINITIONS

STATUS: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

1 = COLD START, NO HISTORY
1 = CHARGE IN PROGRESS
1 = DEEP CYCLE IN PROGRESS
1 = LOW RESERVE CONDITION
1 = LOW VOLTAGE CONDITION
1 = IMPROPER CHARGE VOLTAGE
1 = CHARGE CYCLE INCOMPLETE
1 = MINIMUM CAPACITY ALERT

ANALOG VALUES:

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 8-BIT VALUES SCALED BY BATTERY PROCESSOR AS FOLLOWS:

CH. 0 : CHARGE VOLTAGE, 80 mV/STEP, 20.4 VOLTS MAX

CH. 1: DISCHARGE CURRENT, 2 ma/STEP, 510 ma MAX

CH. 2: BATTERY TERMINAL VOLTAGE, 25 mV/STEP, 6.375 VOLTS MAX

CH. 3 : BATTERY TERMPERATURE, 2°K/STEP (ABSOLUTE)

LOW RESERVE ALERT POINT:

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

8-BIT VALUE, 1 $\leq$ LOW RESERVE ALERT POINT $\leq$ 99

DEFAULT VALUE: 20 = 14(HEX) (20% RESERVE)

SCALED BY BATTERY PROCESSOR AS % C REMAINING WHEN LOW RESERVE INTERRUPT GIVEN TO TERMINAL PROCESSOR

LOW VOLTAGE ALERT POINT:

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

8-BIT VALUE, 0 $\leq$ LOW VOLTAGE ALERT POINT $\leq$ 255

DEFAULT VALUE 190 = 0BE(HEX) (4.75 VOLTS)

SCALED BY BATTERY PROCESSOR AS 25 mV/STEP

TABLE B - (cont.)

MINIMUM CAPACITY ALERT:

7	6	5	4	3	2	1	0

8-BIT VALUE, $0 \leq$ MINIMUM ALERT ≤ 255

10 ma - HR/STEP, 2550 ma - HR MAX.

DEFAULT VALUE: 0 (ESSENTIALLY DISABLED)

WHEN MAXIMUM AVAILABLE CAPACITY (AS MEASURED BY DEEP CYCLE FUNCTION) DECREASES TO THIS LEVEL, AN INTERRUPT ALERT IS GIVEN TO THE TERMINAL PROCESSOR.

MAXIMUM AVIALABLE CAPACITY (C):

7	6	5	4	3	2	1	0

8-BIT VALUE, $0 \leq C \leq 255$

10 ma - HR/STEP, 2550 ma - HR MAX.

MEASURED AND SET DURING DEEP DISCHARGE FUNCTION

DEFAULT VALUE: 100 = 64(HEX)

CHARGE CYCLE COUNT:

BYTE 1 (MS)	7	6	5	4	3	2	1	0
BYTE 0 (LS)	7	6	5	4	3	2	1	0

16-BIT VALUE, INITIALIZED TO 0

COUNTS NUMBER OF CHARGE CYCLES INITIATED

DEEP CYCLE COUNT:

BYTE 1 (MS)	7	6	5	4	3	2	1	0
BYTE 0 (LS)	7	6	5	4	3	2	1	0

16-BIT VALUE, INITIALIZED TO 0

COUNTS NUMBER OF DEEP DISCHARGE-RECHARGE CYCLES

TABLE B - (cont.)

ACCUMULATED HOURS:

BYTE 1 (MS) | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

BYTE 0 (LS) | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

16-BIT VALUE, INITIALIZED TO 0

COUNTS ACTUAL HOURS OF USE DELIVERING CURRENT

USE HISTORY INFORMATION: (4 BYTES)

BYTE 3 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

8-BIT VALUE, COUNTS NUMBER OF TIMES OVER VOLTAGE ON CHARGE EXPERIENCED

BYTE 2 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

8-BIT VALUE, COUNTS NUMBER OF TIMES TEMP EXCEEDED 45°C DURING CHARGE

BYTE 1 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

8-BIT VALUE, AVERAGED DEPTH OF DISCHARGE DURING USE, %C

BYTE 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

8-BIT VALUE, CHANGE IN AVAILABLE CAPACITY FROM MAXIMUM OBSERVED

FUEL GAUGE:

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

8-BIT VALUE, $0 \leq$ FUEL GAUGE VALUE ≤ 100 SCALED BY BATTERY PROCESSOR AS % C REMAINING

Referring to the STATUS word of Table B, for a new battery pack for example, for which no prior history has been recorded, bit zero of the STATUS word would be placed in a logical one condition representing a cold start of battery history. The remaining bits of the STATUS word could be at a logical zero level.

Various of the storage locations represented in Table B have default values which the locations receive in the absence of a particular selected value at the time of start up. For example, a LOW RESERVE ALERT POINT register would be set at a hexadecimal (HEX) value representing an alert point corresponding to a remaining capacity of the battery of 20% of its rated capacity. Thus, in the absence of a different setting, the battery processor would transmit an interrupt to the terminal processor (indicated at 71 in Figure 5) when the battery had been discharged to such an extent that only a 20% reserve of capacity remained.

The CHARGE CYCLE COUNT of Table B, on the other hand, would be initialized to zero.

While the essential features of the invention will be fully understood from the foregoing description, it is proposed to include hereinafter certain further exemplary details concerning a specific implementation of an illustrative overall battery system. It should be understood, however, that the scope of the invention is defined by the claims hereof, and that specific details are given solely by way of example and not by way of limitation. An embodiment of the invention as defined in the claims is readily implemented by one of ordinary skill in the art without reference to the following elaboration.

Applicant would emphasize that the various features of the invention have substantial utility when practiced separately. For example, a non-rechargeable battery system with means for monitoring battery discharge current and automatically alerting the user when battery energy has been reduced to a selected value would have important utility independent of other features. A simplification of the disclosed portable system could be made by utilizing a non-portable system to insert a measured value of battery capacity into the memory of the battery system after each deep discharge cycle. For example the deep discharge and charging cycles might be controlled by a separate non-portable computer system at a central charging station. This computer system might be capable of communication with the memory of the battery system for inserting an accurate actual measurement of battery capacity. For the case of a central computer controlled charging station, the central computer could interrogate the memory of the battery system for relevant battery history and then selectively determine a suitable charging voltage and charging current. At selected times, the central computer could determine that the battery should be fully charged and then deep discharged to measure its actual capacity.

CL U/C Description of Figure 11

P Figure 11 is a flow chart showing the general control program for the battery processor. During start of the system as represented by block 11-1 various storage locations of the memory of component 82, Fig. 5, may be initialized.

With respect to decision block 11-2, the battery processor, for example, may interrogate the battery charging voltage monitor 103, Fig. 5, to determine if a charging voltage is present. If a charging voltage is present, control branches as indicated at 11-3 and 11-4 to obtain the optimum value of battery charging current. Otherwise as represented by blocks 11-5 and 11-6, the battery processor effects the monitoring of battery parameters so as to update the battery information of Table B at suitable intervals.

As represented by decision block 11-7, upon receipt of an interrupt, the battery processor determines if the source of the interrupt signal was the battery processor timer, in which case control returns to decision block 11-2. On the other hand if the source of the interrupt signal was a communication from the keyboard 11 of terminal device 10, processing continues as indicated at 11-8. The respective command types pursuant to blocks 11-9 through 11-11 correspond to the respective code groups of Table A. Following execution according to block 11-11, the control program returns to block 11-2.

CL U/C Description of Tables C and D

P Exemplary circuit components and resistance and capacitance values for Figs. 9A and 9B are shown in the following TABLES C and D.

TO400X

TABLE C (FIG. 9A)

Comparator 172	LM10B
Transistors T_1, T_2, T_3	ZTX750
Resistors R_a, R_b, R_c	2.2 kilohms, each
Schottky Diodes D_1, D_2, D_3	IN5819
Circuit 180	Darlington NPN
Resistors 182	47 ohms, 1/2 watt, each
Resistor 132	32.4 kilohms, 1%
Resistor 133	10 kilohms, 1%
Transducer 134	AD 590
Battery 20	2.2 ampere hour four cells x 1/2 D Polytemp Nickel-Cadmium
Resistor 131	.1 ohm, 1%
Amplifier of 170	CA 3260
Resistor R_d	29.4 kilohms, 1%
Capacitor C_a	.1 microfarad
Resistor R_e	1 kilohm, 1%
Amplifier 176	CA 3260
Resistor R_f	57.6 kilohm, 1%
Capacitor C_f	.1 microfarad
Resistor R_i	1 kilohm, 1%
Resistor 135	2.94 kilohm, 1%
Resistor 136	127 kilohms, 1%
Resistor 137	10 kilohms, 1%
Comparators 151-154	LM 339

T0410X

TABLE D (FIG. 9B)

Voltage Regulator 150	LM10B
Resistor R_1	10 kilohms, 1%
Resistor R_2	140 kilohms, 1%
Crystal 196	1 megahertz
Resistor R_3	10 megohms
Resistors R_4, R_5, R_6, R_8	100 kilohms each
Resistor R_7	20 kilohms
Comparators 191-193	LM 339
Resistors R_9, R_{10}, R_{11}	100 kilohms each
Comparator 195	LM 339
Resistor R_{12}	100 kilohms
Capacitor C_1	.1 microfarad
Resistor R_{13}	10 kilohms, 1%
Resistor R_{14}	127 kilohms, 1%
Resistors R_{15-18}	100 kilohms, each
R Resistance Values	100 kilohms, 1%, each
2R Resistance Values	200 kilohms, 1%, each
Resistor R_{19}	10 kilohms
Processor Circuit 140	MC 146805F2

CL 4C Description of FIG. 12

P Fig. 12 illustrates a simplified embodiment of a portable battery powered system in accordance with the present invention. Reference numeral 12-10 represents a portable utilization device which may have the same appearance and characteristics as described for the device 10 shown in Fig. 1. Thus the device 12-10 may have a terminal display circuit 12-12 associated with a display region such as indicated at 12 in Fig. 1 and may include processor and memory circuits 12-14 including a microprocessor located generally as indicated at 14 in Fig. 2. Battery charge and deep discharge controller and battery condition monitor circuitry 12-18 could correspond with the circuitry previously described in Figs 5, 9A and 9B, with the difference that the circuitry is permanently associated with the portable device 10 and is located in a space adjacent to space 14 of Fig. 2 rather than being a permanent part of the battery pack as indicated in Figs. 3 and 4. Thus, in the embodiment of Fig. 12 a rechargable battery means is indicated at 12-20 and may comprise four nickel-cadmium cells supplying a nominal output voltage of five volts and having the characteristics previously described including those indicated in Figs. 6, 7 and 8. In the simplified embodiment of Fig. 12, however, the rechargable battery means 12-20 is readily detachable from the circuitry 12-18 so as to be removable and replaceable without disturbing circuitry 12-18. By way of example circuitry 12-18 may be installed on a separate board which fits within the housing of the device 10 of Fig. 1 in the same way as the microprocessor board located at 14 in Fig. 2. In Fig. 12, small circles have been applied to represent a quick disconnect coupling between components 12-14 and 12-18. Thus, the terminal conductors of component 12-14 may be

readily disconnected at 12-21 from the circuitry 12-18 and connected instead to output devices such as indicated at 51 in Figs. 2 and 5, so that components 12-12 and 12-14 may be readily adapted to cooperate with the battery system of Figs. 3 and 4 including the circuitry of Figs. 9A and 9B.

For the simplified embodiment of Fig. 12, conventional spring type coupling has been indicated at 12-22 between circuitry 12-18 and battery means 12-20, so that a conventional battery pack is automatically coupled with the circuitry 12-18 when inserted into the portable device 12-10. By way of example, device 12-10 may correspond essentially to a portable data terminal of Norand Corporation identified as the NT 121 data terminal, modified to include component 12-18 and receiving a conventional nickel cadmium battery pack by means of a releasable coupling at 12-22 corresponding to that utilized in the commercial device. In the commercial system, the battery pack may be charged by coupling of component 12-14 to a battery charger means such as indicated at 12-24, for example by means of a plug and socket coupling indicated at 12-25. Component 12-14 when associated with a battery charger means may supply a charging voltage output
30 (+CHG) as indicated in association with terminal 44 in Fig. 5,
30 while component 12-14 may receive battery output voltage (V+, ground) from the battery means 12-20 via circuitry 12-18, as indicated in association with terminals 45 and 46 in Fig. 5. In an embodiment corresponding to that previously described, circuitry 12-18 would correspond to components 81, 82, 83, 91, 92, 93, 101, 103 and 110 of Fig. 5, for example. In a simplified specific embodiment, component 12-18 may utilize circuitry such as illustrated in Fig. 13.

Cl. ½ Description of FIG. 13

Fig. 13 illustrates a specific battery charge and deep discharge controller and battery condition monitor circuit corresponding to component 12-18 of Fig. 12. The circuit 13-10 of Fig. 13 may be implemented as a printed circuit board for insertion into the previously mentioned model 121 portable data terminal such as illustrated in Fig. 1. For the sake of correlating the circuit of Fig. 13 with the illustration of Fig. 12, the terminals at the right hand side in Fig. 13 have been designated 12-21a through 12-21f to indicate there correlation with the quick disconnect coupling indicated at 12-21 in Fig. 12 between components 12-14 and 12-18.

For the specific commercial device previously identified, terminal 12-21a receives charging current of .66 amperes from a constant current circuit of component 12-14 which ~~intern~~ in turn is energized from battery charger means 12-24. Terminal 12-21a is thus designated by the notation "CHARGE". S.E.K 5-17-84

Terminal 12-21b at the right in Fig. 13 receives a logical control signal from component 12-14. For example, with terminal 12-21b in a high potential condition, the charging current through transister Q9 is at a value corresponding to rated capacity in ampere hours divided by 8.3 hours (C/8.3 amperes). With terminal 12-21b at a low logical potential level, the charging current has a value of full capacity divided by 100 (C/100). Switch 13-11 provides over temperature protection and may operate at a temperature 55 degrees centigrade.

S.E.K. 5-17-84 S.E.K. 5-17-84

Comparator 13-12 may sense an over-voltage condition and may receive a reference input of 2.000 volts at its upper inverting input.

Terminal 12-21b is designated by the legend "CHARGE CONTROL" and may be controlled from the programmed processor of component 12-14.

S.E.K. 5-17-84

Battery 12-20 has been indicated in Fig. 13 operatively engaged with coupling elements which are indicated at 12-22a and 12-22b. The battery 12-20 is coupled by a terminal 12-21c and 12-21d with the component 12-14 for supplying operating power to the portable device during normal operation thereof.

Terminals 12-21e and 12-21f are utilized to effect an automatic deep discharge cycle. When terminal 12-21f is at a logical low potential state, terminal 12-21e provides a signal LB1 which in the high logical potential condition represents a low battery condition as sensed by comparator 13-14.

When terminal 12-21f is at a logical high potential condition, transistor Q7 is turned on, so as to activate the constant current discharge circuit including component 13-15. By way of example, the discharge of battery 12-20 may be at a rate of full capacity divided by five hours (C/5 amperes). During discharge operation, comparator 13-20 is active and provides a logical high potential signal (LB2) when a discharge value of battery potential, for example 3.8 volts, has been detected. For the specific battery referred to, comparator 13-12 may be activated at a voltage value of 6.2 volts, and then be reset when battery voltage is reduced to a value of 5.4 volts. Comparator 13-14 may be activated at a low battery voltage value of 4.65 volts, and be reset when the battery 12-20 has been charged above a voltage value of 5.4 volts. Comparator 13-20 may be activated at a discharge voltage value of 3.8 volts and then be reset when the battery 12-20 has been recharged to a voltage value above 5.4 volts, for example.

Terminal 12-21e is designated with the legend "LB1/LB2) and the terminal 12-21f is labeled with the legend "DISCHARGE".

By way of example, it will be apparent that the system of Fig. 12 may serve as a stationary battery conditioning system for removably receiving spare battery packs. Such a system could correspond to that illustrated in Fig. 1, but with the housing of device 10 permanently fastened to a stationary supporting frame. Conveniently, a removable cover such as 17 could be replaced by a quick access lid with a simple hinge, or the battery space for a conventional battery pack could be simply left open. Of course, a corresponding circuit could be made with heavier parts of the like specifically for stationary operation.

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CL 46 Description of Fig. 14

P Fig. 14 illustrates exemplary automatic operation of the system of Figs. 12 and 13 in conducting a test of battery capacity. When a portable system 12-10 is plugged into battery charger means 12-24, a deep discharge and recharge of the battery may be carried out. Such a procedure should be performed at least once a month to maintain the storage capacity of the battery. With the battery 12-20 fully recharged, a capacity measurement function as indicated in FIG. 14 may be performed when convenient. In the illustrated embodiment, the result of the capacity test is an indication of a percentage equal to the discharge time observed during a deep discharge cycle divided by eight hours. A value exceeding eighty percent may indicate that the batteries are still functioning adequately.

Referring to Fig. 14, a capacity test may be initiated by pressing the ENTER KEY, Fig. 1, in response to the prompt CAPACITY TEST? appearing at the display 12. By way of example, this prompt may appear once a conditioning discharge of the battery has been completed. Alternatively, selection of the capacity test function may automatically cause the battery to be discharge and fully charged before the actual capacity test steps of Fig. 14 are automatically carried out. In this case, step 14-2 might read: BATTERY DEEP DISCHARGED AND FULLY RECHARGED?

In the illustrated embodiment, step 14-2 may correspond with waiting until a battery charge timer indicates full charge by decrementing to zero from 780 minutes.

Once the battery is fully recharged, the operating system reads the current time as a starting time for the deep discharge cycle.

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According to step 14-4, component 12-14 supplies a logical high potential signal to terminal 12-21f, Fig. 13 to initiate a further deep discharge cycle.

In executing step 14-5, the operating system of component 12-14 monitors terminal 12-21e of Fig. 13 for a logical high potential signal indicating that the battery has been discharged to a discharge level of for example 3.8 volts.

According to step 14-6, when a logical high potential signal appears at terminal 12-21e, the current time is read from a clock of component 12-14 as the "LB2 TIME".

By step 14-7, a logical low potential signal is supplied to terminal 12-21f to turn off the discharge circuit, and a logical high potential signal is supplied to terminal 12-21b to initiate a fast recharge of the battery.

For step 14-8, the processor of component 12-14 obtains the difference between the LB2 TIME and the starting time, as a measure of the time required for the deep discharge cycle. Where with a battery in good condition the deep discharge cycle requires eight hours, the calculation of step 14-8 obtains the percentage value of the observed deep discharge time in comparison to a discharge time of eight hours.

Pursuant to step 14-9, component 12-14 may cause the calculated deep discharge time to be displayed at the display means 12 of Fig. 1. For example, if the observed deep discharged S.E.K.
32 time were six hours, the display might show: "BATT PERCENT = 75". 5-17-8

An outline of a battery discharge subroutine (PSBAT1P) for the commercial model 121 portable data terminal is set forth on the following pages, followed by a program listing of this subroutine.

CL 4/ Description of an Exemplary Computer Program for an Embodiment According to FIGS. 12-14

A battery discharge program has been written and is in use for the model 121 portable data unit which has been described in connection with FIGS. 12-14 of the present drawings.

The system as represented in FIG. 12, comprises operating means including a NSC-800 processor and real time clock, automatically operating according to FIG. 14 under the control of the subroutine which is known as PSBAT1P. A copy of user guide specification for this subroutine is as follows:

Copy of User Guide Specification for the Subroutine PSBAT1P

SUBROUTINE: PSBAT1P

This subroutine has no parameters. In order to access it, it must be declared in the EXTERNALS section of a program, and then linked to the program, according to the conventions of the development system.

General Description

PSBAT1P is a PL/N battery discharge subroutine written for the NT121 data terminal. This subroutine performs two functions:

(1) It performs a deep discharge and recharge of the terminal.

(2) It measures the storage capacity of the NICAD batteries by timing the time required to discharge the batteries when fully charged.

The capacity test takes twice as long to execute as the simple discharge and recharge function. This is because the batteries must be discharged and charged before the actual capacity test can be performed. The result of the capacity time is a percentage equal to the discharge time divided by eight hours. A value exceeding 80% indicates the batteries are still functioning adequately.

The deep discharge and charge function should be performed at least once a month to maintain the storage capacity of the batteries. The capacity measurment function may be performed when convenient.

It is required that the NT121 remain on charge while the subroutine is executing. If it is taken off charge, an error message will be displayed and program execution will stop. Volatile data in the 121 will be maintained during the deep discharge provided that the unit is not taken off charge while in the low battery mode.

C1. Power-up

When IPSDISP has been called from a main program the following message will be seen in the display:

Prompt: BATT. DISCHARGER
IPSDISP Vx.x

Action:

Press <ENTER> to proceed or press <SKIP> to halt program execution and return to the monitor program.

Prompt: EXIT PROGRAM?

Action:

Press <ENTER> if it is desired that program execution is to be terminated or press <SKIP> to proceed.

Prompt: CAPACITY TEST?

Action:

To measure the capacity of the batteries, press <ENTER>. Press <SKIP> if this is not desired.

Prompt: CURR TIME:hhmmss

Action:

The current time is displayed in HHMMSS format. If no change in the time is desired just press <ENTER>. Otherwise enter the desired time in HHMMSS format. No mod checks are performed on this newly entered time. Make sure that the unit is on charge. This test will terminate if the 121 is removed from and not placed back on charge within 30 seconds.

Prompt: RCHRG TIME:nnnnn

This prompt will appear only when the capacity test has been selected. The contents of the battery charge timer will be displayed and updated every 5.5 seconds until its value is zero (full charge). The value of the RTC will be read and stored. This test will terminate if the 121 is removed from and not placed back on charge within 30 seconds.

P

Prompt: DISCHARGING.

P This prompt indicates the 121 is currently discharging its batteries. This will continue until LB2 becomes active (batteries discharged). The LOW BATT flag on indicates that the unit is discharging and the blinking SHIFT flag indicates the unit is active. This test will terminate if the 121 is removed from and not placed back on charge within 30 seconds.

P **Prompt: RECHARGING.**

P This prompt indicates that the 121 has reached LB2. The value of the RTC is then read and saved. The unit will start to charge its batteries until LB1 becomes inactive (not low battery). The blinking SHIFT flag indicates the unit is active. When LB1 becomes inactive the RTC is then read and saved. This test will terminate if the 121 is removed from and not placed back on charge within 30 seconds.

P **Prompt: S TIME: hhmmss**

P **Action:**

The 121 no longer checks if it is on charge. It is the user's responsibility to ensure that the unit remains on charge until the LOW BATT flag is turned off in order for the batteries to fully benefit from this test. The time stored at the beginning of the test is displayed in HHMMSS format. Press <ENTER> to proceed. 21 22

P Prompt: LB2 TIME: hhmmss

P **Action:**

The time where LB2 became active is displayed. Press <ENTER> to proceed. 21 22

P Prompt: LB1 TIME: hhmmss

P **Action:**

The time where LB1 became inactive is displayed. Press <ENTER> to continue. 21 22

Prompt: % CAPACITY: nnn

Action:

This prompt will appear only if the capacity test was selected. It is a percentage of:

(time taken to discharge the batteries from a full charge) / eight hours.

Press <ENTER> to proceed.

When either the capacity or conditioning tests are executing and the 121 is removed from charge the following message will be displayed.

Prompt: CHARGER!

Action:

If the unit is placed back on charge within 30 seconds the test will continue. If it is not an error message will be displayed.

Prompt: TEST ABORTED.

Action:

Press <ENTER> to proceed to the 'EXIT PROGRAM?' prompt.

Introduction to the Listing of the Subroutine PSBAT1P

The following listing has the heading:

"PSBAT1P: 121 BATTERY DISCHARGE & CYCLE PLN VER 2.8 03/23/84 12:41: 49", and is generally outlined as follows:

0-5 "$ PSBAT1P; 121 BATTERY DISCHARGE & CYCLE SUBROUTINE PSBAT1P

VERSION 0016"

6-28; HISTORY

07/07/83 ; Under this data a first programmer is shown as author of a program entitled "121 BATTERY DISCHARGE PROGRAM"

07/13/83 ; "REMOVED THE CODE THAT ALLOWED THE USER TO MODIFY THE BATTERY CHARGE TIMER."

08/01/83 ; Under this data a second programmer has the note: "PSBAT1P CREATED"

11/21/83 ; On November 21, 1983, there is a notation by a third programmer "COPY FILE PCURCNP CHANGED, THIS CODE WAS FIXED TO REFLECT THE CHANGES. REMOVED PROGRAM HEADER,"

03/23/84 ; On March 23, 1984, a fourth programmer makes the following entry into the program history:

"MODIFIED SO THAT THE SYSTEM DRIVER IS NOT NEEDED. IT WAS ONLY USED TO DETERMINE WHEN FULL CHARGE WAS ACCOMPLISHED. THIS IS NOW DONE BY DETERMINING IF THE INTERPRETER IS CURRENTLY CHARGING THE BATTERIES. IF NOT, TEST TO SEE IF IT IS BECAUSE THE CHARGE POWER HAS BEEN REMOVED. IF IT HAS NOT, THEN THE PRECHARGE IS COMPLETE. THE DISPLAY OF TIME NOW INCREMENTS BY TENTHS INSTEAD OF DECREMENTS BY MINUTES."

29-33	EXTERNALS	NUMERIC FUNCTION INPUT
34-45	PSBAT1P	PROGRAM CONSTANTS
46-72	PCINCNP	INPUT CONTROL ATTRIBUTES
74-101	PCHRCNP	CHARACTER AND KEY DEFINITIONS
102-152	PCKBCNP	KEYBOARD OPEN MODES, GET AND PUT CONTROL OPTIONS
153-200	PCURCNP	URTIO GET AND PUT CONTROL
207-200	PCKBCMP	REQUIRED IF 'INPUT' FUNCTION AND/OR 'PRINT' SUBROUTINE ARE LINKED WITH APPLICATION
227-249	PCLKFDP	CLOCK FD AND BUFFER
306-341	PROCEDURE	BATT TEST
342-421	PROCEDURE	DEEP DISCHARGE
422-449	PROCEDURE	PLUG IN CHARGER

CL U/C Excerpts of Detailed Listing of Subroutine PSBAT1P

P A copy of the listing (except for locations 1-33 which are adequately indicated in the proceding section) is as follows:

```
0   $ PSBAT1P PROGRAM CONSTANTS
0     CONSTANTS
0
0       VER                        = 'V1.5'
0       TRUE                       = 1
0       FALSE                      = 0
0       MINUS_ONE                  = 65535
0       SPACE                      = 32
0       UNDERSCORE                 = 95
0       HI_VALU                    = 255
0       NULL                       = 0
0
```

```
    0 $
    0
    0   ;BEGIN COPY LIBRARY - PCINCNP
    0
    0   ;*****************************************************************
    0   ;
    0   ;   'INPUT' CONTROL ATTRIBUTES
    0   ;
    0   ;*****************************************************************
    0
    0   E     = 0      ;ENTER ONLY
    0   S     = 1      ;SKIP ALLOWED
    0   F     = 2      ;FUNCTION ALLOWED
    0   A     = 8      ;AUTO-ENTRY ALLOWED
    0   V     = 36     ;VIEW WITHOUT DATA ENTRY
    0   VD    = 68     ;VIEW WITH UPDATE AFTER A DELETE
    0   VDO   = 20     ;VIEW WITH OPTIONAL UPDATE
    0   SCR   = 128    ;SCROLL
    0   T     = 256    ;PROMPT ON THE TOP LINE
    0   B     = 512    ;PROMPT ON THE BOTTOM LINE
    0   H     = 1024   ;HOME THE CURSOR AND CLEAR DISPLAY
    0   L     = 2048   ;ALLOW SEARCH
    0   N     = 4112   ;CLEAR INPUT FIELD ON ENTER ONLY
    0   TB    = 8192   ;PROMPT ON TOP, INPUT ON BOTTOM
    0   RTD   = 16384  ;RETURN ON DELETE/CLEAR AND CHRCNT = 0
    0   RTF   = 32768  ;RETURN ON CONTROL KEY
    0    ,
    0   ;END COPY LIBRARY - PCINCNP
```

```
0 $
0
0   ;BEGIN COPY LIBRARY - PCHRCNP
0
0   ;**************************************************
0   ;
0   ; CHARACTER AND KEY DEFINITIONS
0   ;
0   ;**************************************************
0   BEL            = CHAR (7)      ;BEEP
0   BS             = CHAR (8)      ;BACKSPACE
0   LF             = CHAR (10)
0   CR             = CHAR (13)
0   CRLF           = CR & LF
0   SP             = CHAR (32)     ;SPACE
0   HT             = CHAR (9)      ;HORIZONTAL TAB
0
0   FUNC_KEY     = 6
0   SKIP_KEY     = 27
0   ENTER_KEY    = 13
0   UP_KEY       = 8
0   DOWN_KEY     = 10
0   SRCH_KEY     = 12
0   DEL_KEY      = 127
0   CLR_KEY      = 21
0       ,
0   ;END COPY LIBRARY - PCHRCNP
```

```
0  $
0
0    ;BEGIN COPY LIBRARY - PCKBCNP
0
0    ;*****************************************************
0    ;
0    ;  KEYBOARD OPEN MODES, GET AND PUT CONTROL OPTIONS
0    ;
0    ;*****************************************************
0
0    KB_NAME        = 'KBDIO:'
0
0    ;OPEN MODES
0
0    KB_KEY_CLICK  = 1        ;OPEN WITH KEY CLICK ON
0    KB_SHIFT_LOCK = 2        ;OPEN WITH SHIFT LOCK ON
0    KB_OFF_CURSOR = 4        ;OPEN WITH CURSOR OFF
0
0    ;GET CONTROL
0
0    KB_CHRCNT     = 1        ;GET NUMBER OF CHARS INPUT
0    KB_KEY        = 2        ;GET LAST KEYPRESS
0    KB_LCD        = 3        ;GET LCD ATTRIBUTES
0
0    ;PUT CONTROL
0
0    KB_PARTIAL    = 768      ;PARTIAL FORMATTING
0    KB_FULL       = 769      ;FULL FORMATTING
0    KB_AUTO       = 770      ;AUTO ENTRY ON
0    KB_NOAUTO     = 771      ;AUTO ENTRY OFF
0    KB_NOENTRY    = 772      ;NO DATA ENTRY REQUIRED
0    KB_ENTRY      = 773      ;DATA ENTRY REQUIRED
0    KB_ABORT      = 774      ;ALLOW CONTROL KEYS TO EXIT INPUT
0    KB_NOABORT    = 775      ;DON'T ALLOW
0    KB_BUZZER     = 1033     ;TURN ON DISPLAY BUZZER
0    KB_OFFBUZZER  = 1034     ;TURN OFF DISPLAY BUZZER
0    KB_CURSOR     = 1280     ;TURN CURSOR ON
0    KB_NOCURSOR   = 1281     ;TURN CURSOR OFF
0    KB_HOME       = 1282
0    KB_CLEOL      = 1283     ;CLEAR TO END OF LINE
0    KB_CLEOF      = 1284     ;CLEAR TO END OF PAGE
0    KB_SWAP       = 1285     ;SWAP KEY TABLES
0    KB_CLICK      = 1286     ;KEY CLICK ON
0    KB_NOCLICK    = 1287     ;KEY CLICK OFF
0    KB_LOCK       = 1288     ;LOCK KEYBOARD
0    KB_UNLOCK     = 1289     ;UNLOCK KEYBOARD
0    KB_BINARY     = 1290     ;SEND BINARY DATA TO PORT
0    KB_WIDTH      = 1291     ;SET CHARACTERS PER ROW
0    KB_LENGTH     = 1292     ;SET NUMBER OF ROWS
0
0    ;END COPY LIBRARY - PCKBCNP
```

```
0 $
0
0  ;BEGIN COPY LIBRARY - PCURCNP
0
0  ;***************************************************************
0  ;
0  ;  URTIO GET AND PUT CONTROL
0  ;
0  ;***************************************************************
0
0  ;GET CONTROL
0
0  UR_CHRCHT        = 1      ;CHARACTERS RETURNED BY LAST IN
0  UR_KEY           = 2      ;LAST CHARACTER RETURNED
0  UR_SIGNALS       = 5      ;EIA/BATTERY SIGNALS
0
0  ;PUT CONTROL
0
0  UR_BAUD          = 2048   ;SET BAUD RATE
0  UR_PARITY        = 2050   ;SET PARITY
0  UR_DATA          = 2051   ;SET NUMBER OF DATA BITS
0  UR_STOP          = 2052   ;SET NUMBER OF STOP BITS
0  UR_ROUTE         = 2053   ;SET IO ROUTING
0  UR_SET           = 2054   ;ACTIVATE THE IO PINS
0  UR_RESET         = 2055   ;DEACTIVATE
0  UR_TIME1         = 2060   ;1ST CHARACTER WAIT TIME
0  UR_TIME2         = 2061   ;INTERCHARACTER WAIT
0
0  ;PINS
0
0  UR_DTR           = 1
0  UR_RTS           = 2
0  UR_RCT           = 4
0  UR_TXD           = 8
0  UR_SCAN          = 16
0  UR_BACKUP        = 32     ;BACKUP BATTERY
0  UR_CHRG_CNTL     = 64     ;TRICKLE  = 0, FULL = 1
0  UR_DISCHARGE     = 128    ;DISABLED = 0 (LB1), ENABLED = 1 (LB2)
0  UR_DSR           = 256
0  UR_CTS           = 512
0  UR_RCR           = 1024
0  UR_RXD           = 2048
0  UR_PROXIMITY     = 4096
0  UR_CROSSOVER     = 8192
0  UR_LOWBATT       = 16384  ;LB1/LB2
0  UR_CHARGE        = 32768  ;CHARGER PLUGGED IN = 1
0
0  ;END OF COPY LIBRARY - PCURCNP
0       CHARGE_CNTL                = 64    ;FAST/TRICKLE CHARGE
0       DISCHARGE                  = 128   ;DEEP DISCHARGE
```

```
0  $ PSBATIP PROGRAM FD'S AND BUFFERS
0
0    COMMON VARIABLES
0
0    ;BEGIN COPY LIBRARY - PCKBCMP
0
0    ;*****************************************************************
0    ;
0    ;  FIXED COMMON AREA
0    ;
0    ;  - REQUIRED IF 'INPUT' FUNCTION AND/OR 'PRINT' SUBROUTINE ARE
0    ;    LINKED WITH APPLICATION
0    ;
0    ;*****************************************************************
0
0    FD              KBD
0    01 KEY          BINARY BYTE    ;HOLDS MOST RECENT KEYPRESS
0    01 CHRCNT       BINARY BYTE    ;HOLDS NUMBER OF CHARS INPUT
0    FD              PRT (56)       ;53 CHARS + 3 FOR NEW PROTOCOL SUPPORT
0  ; FD              PRT            ;OLD PROTOCOL
0
0    ;END COPY LIBRARY - PCKBCMP
0
0
0     ;BEGIN COPY LIBRARY - PCLKFDP
0
0     ;*********************************************************
0     ;
0     ;  CLOCK FD AND BUFFER
0     ;
0     ;*********************************************************
0
0     FD                     CLK
0     01 CLKBUF
0        05 TIME
0           10 HOURS                       PIC 99
0           10 MINS                        PIC 99
0           10 SECS                        PIC 99
0        05 SHOW_TIME REDEFINES TIME       PIC X(6)
0        05 DATE
0           10 YEAR                        PIC 99
0           10 MONTH                       PIC 99
0           10 DAY                         PIC 99
0        05 SHOW_DATE REDEFINES DATE       PIC X(6)
0        05 DAY_OF_WEEK                    PIC 9      ;SUNDAY = ONE
0
0     ;END COPY LIBRARY - PCLKFDP
0      01  ASGNCLK REDEFINES CLKBUF      PIC 9(6)
0
0    LOCAL VARIABLES
0
0      FD  URT
0      FD  SYS
0
0      01  KBD_BUFFER                      PIC X(32)
```

```
258      0
259      0      01  KBD_SAVE                   PIC X(32)
```

```
0   $ PSBAT1P PROGRAM PROGRAM VARIABLES
0
0      01  PROG_VARIABLES
0          05  RESPONSE                      PIC 9
0          05  DSP_SIZE                      BINARY BYTE
0          05  KK                            BINARY BYTE
0          05  M                             BINARY WORD
0          05  BATT_PERCENT                  PIC ZZ9
0          05  STRT_TIME                     PIC 9(6)
0          05  RSTRT_TIME REDEFINES STRT_TIME
0              10  HRS                       PIC 99
0              10  MINS                      PIC 99
0              10  SECS                      PIC 99
0          05  LOW_TIME                      PIC 9(6)
0          05  RLOW_TIME REDEFINES LOW_TIME
0              10  HRS                       PIC 99
0              10  MINS                      PIC 99
0              10  SECS                      PIC 99
0          05  END_TIME                      PIC 9(6)
0          05  CURR_EIA                      BINARY WORD
0          05  SAVE_EIA                      BINARY WORD
0          05  RSAVE_EIA REDEFINES SAVE_EIA
0              10  SAVE_HIGH                 BINARY BYTE
0              10  SAVE_LOW                  BINARY BYTE
0          05  BATT_TIME                     PIC ZZNVN
0          05  DEBOUNCE_CHARGER              BINARY BYTE
```

```
 0  $ PSBATIP PROGRAM MASTER_CONTROL
 0  ;  OPEN DRIVERS, FILES AND INIT ERROR PROCEDURES
 0
 0    PROCEDURE INIT
 0     ;OPEN(KBD,KBD_BUFFER)'KBDIO!',KB_KEY_CLICK + KB_OFF_CURSOR
 0                                                             ;OPEN DRIVERS CURSOR OFF
 0     ;GETCTL(KBD) DSP_SIZE, KB_LCD                           ;LED OR LCD DISPLAY?
 0     ;PUTCTL(KBD) 16, KB_WIDTH,  DSP_SIZE/16, KB_LENGTH      ;LINE_LENGTH 16 CHAR ROW
 0      OPEN(CLK,CLKBUF)'CLKIO!'
 6      OPEN(URT)'URTIO!'
12      PERFORM MASTER_CONTROL
14    END;  END INIT
```

```
PSBAT1P PROGRAM MASTER_CONTROL                              PLN VER 2.8  03/23/84 12:41:49  PAGE  12

      15  $
      15    PROCEDURE MASTER_CONTROL
      15  ;
      15      WHILE (INPUT(H+S,'BATTERY TEST?')) DO
      24        PERFORM BATT_TST
      26      ENDWHILE
      28  ;   STOP
      28    END;  END MASTER_CONTROL
```

```
 29  $
 29    PROCEDURE BATT_TST
 29  ;
 29  ;        THIS PROCEDURE ALLOWS THE USER TO SELECT THE BATTERY
 29  ;        CAPACITY TEST OR NOT.  IF THE CAPACITY TEST IS CHOSEN
 29  ;        THIS PROCEDURE WILL WAIT UNTIL THE BATTERY CHARGE
 29  ;        TIMER HAS REACHED FULL CHARGE (DECREMENTED TO ZERO
 29  ;        FROM 780 MINUTES) BEFORE DISCHARGING IS INITIATED.
 29  ;
 29     M = INPUT(H+S,'CAPACITY TEST?')
 38     GET(CLK)                                  ;READ START TIME
 40     RESPONSE = INPUT(VDO+H,'CURR TIME!',ASGNCLK)
 50     IF CHRCNT <> 0 THEN PUT(CLK)
 55  ;*
 55  ;*   CHARGE TILL BATTERY TIMER = 0 FOR CAPACITY TEST.
 55  ;*
 55     IF M THEN
 58       DEBOUNCE_CHARGER = 10
 62       REPEAT
 62         GETCTL(URT) CURR_EIA, UR_SIGNALS
 66         IF (CURR_EIA AND CHARGE_CNTL) THEN
 72           OUT(KBD)(KB_HOME)'RCHRG TIME!',BATT_TIME
 81           WAIT 60                               ;WAIT FOR TIMER
 84           BATT_TIME = BATT_TIME + 0.1
 90           DEBOUNCE_CHARGER = 10
 94         ELSEIF NOT(CURR_EIA AND UR_CHARGE) THEN
103           PERFORM PLUG_IN_CHARGER
105         ELSE
107           DEBOUNCE_CHARGER = DEBOUNCE_CHARGER - 1
112         ENDIF
112       UNTIL DEBOUNCE_CHARGER = 0
116     ENDIF
116     GETCTL(URT) SAVE_EIA, UR_SIGNALS
120     IF NOT(SAVE_EIA AND UR_CHARGE) THEN PERFORM PLUG_IN_CHARGER
129     PERFORM DEEP_DISCHARGE
131    END;
```

```
132  $
132     PROCEDURE DEEP_DISCHARGE
132  ;
132  ;        M IS AN INPUT FLAG THAT INDICATES CAPACITY TEST OR NOT.
132  ;        THIS PROCEDURE WILL DISCHARGE TILL LB2 (DISCHARGED),
132  ;        THEN RECHARGE TILL NOT LB1 (NOT LOW BATTERY).
132  ;        TOGGLE THE SHIFT FLAG TO SHOW ACTIVITY.
132  ;
132  ;        ALLOW THE INTERPRETER TIME TO DO ITS THING.
132  ;        IPMONA WILL SET CHARGE_CNTL (FAST CHARGE) WHEN LB2 IS REACHED.
132  ;
132  ;        WHEN NOT LB1 IS REACHED DISPLAY THE START TIME,
132  ;        LB2 TIME, AND NOT LB1 TIME.  IF THE CAPACITY TEST WAS
132  ;        CHOSEN THE BATTERY CAPACITY WILL THEN BE CALCULATED
132  ;        ON AN 8 HOUR BASE AND THEN DISPLAYED TO THE USER.
132  ;        BATTERY CAPACITY WILL NOT EXCEED 100 PERCENT.
132  ;
132       GET(CLK)                                     ;READ STARTING TIME
134       STRT_TIME = ASGNCLK
137  ;*
137  ;*    TURN ON DISCHARGE, TURN OFF FAST CHARGE FOR MAINS & BACKUP.
137  ;*
137       PUTCTL(URT) DISCHARGE, UR_SET,
137  &                UR_BACKUP+CHARGE_CNTL, UR_RESET ;TURN ON DISCHARGE
147       OUT(KBD)(KB_HOME)'DISCHARGING.'
154       REPEAT
154        'WAIT 55
157         PUTCTL(KBD) KB_LOCK
161         GETCTL(URT) CURR_EIA, UR_SIGNALS
165         IF NOT (CURR_EIA AND UR_CHARGE) THEN
172           PERFORM PLUG_IN_CHARGER
174  ;*
174  ;*    RECOVER FROM IPMONA AFTER TAKEN OFF WALL CHARGER
174  ;*
174           PUTCTL(URT) DISCHARGE, UR_SET,
174  &                    UR_BACKUP+CHARGE_CNTL, UR_RESET
184           GETCTL(URT) CURR_EIA, UR_SIGNALS
188         ENDIF
188         WAIT 10
191         PUTCTL(KBD) KB_UNLOCK
195       UNTIL (CURR_EIA AND UR_LOWBATT) OR (CURR_EIA AND CHARGE_CNTL)
206  ;*
206  ;*    LB2 REACHED (BATTERIES DISCHARGED)
206  ;*                                                  ;READ LB2 TIME
206       GET(CLK)
208       LOW_TIME = ASGNCLK
211  ;*
211  ;*    TURN OFF DISCHARGE, TURN ON FAST CHARGE FOR MAINS & BACKUP.
211  ;*
211       PUTCTL(URT) DISCHARGE, UR_RESET,
211  &                UR_BACKUP+CHARGE_CNTL, UR_SET
221       OUT(KBD)(KB_HOME)'RECHARGING.'
228       REPEAT
228         WAIT 55
231         PUTCTL(KBD) KB_LOCK
```

```
235        GETCTL(URT) CURR_EIA,UR_SIGNALS
239        IF NOT(CURR_EIA AND UR_CHARGE) THEN PERFORM PLUG_IN_CHARGER
248        WAIT 10
251        PUTCTL(KBD) KB_UNLOCK
255      UNTIL ( NOT (CURR_EIA AND UR_LOWBATT))
262   ,*
262   ,*  NOT LB1 REACHED (BATTERIES OUT OF LOW BATT)
262   ,*
262      GET(CLK)                                        ;READ NOT LB1 TIME
264      END_TIME = ASGNCLK
267      RESPONSE = INPUT(H+V,'S TIME!',STRT_TIME)
267   & +           INPUT(V,'LB2 TIME!',LOW_TIME)
267   & +           INPUT(V,'LB1 TIME!',END_TIME)
295      IF M THEN                          ;WAS THIS CAPACITY TEST?
298        IF RSTRT_TIME.HRS > RLOW_TIME.HRS THEN
298   &      RLOW_TIME.HRS = RLOW_TIME.HRS + 24
309        BATT_PERCENT = (((RLOW_TIME.HRS * 3600) + (RLOW_TIME.MINS * 60)
309   &                 + RLOW_TIME.SECS) - ((RSTRT_TIME.HRS * 3600)
309   &                 + (RSTRT_TIME.HRS * 60) + RSTRT_TIME.SECS))
309   &                 / 288        ;288 = 100/(8HRS * 3600)
337        IF BATT_PERCENT > 100 THEN
337   &      BATT_PERCENT = 100
347        RESPONSE = INPUT(H+V,'% CAPACITY!',BATT_PERCENT)
357      ENDIF
357    END;
```

```
350  $
358    PROCEDURE PLUG_IN_CHARGER
358  ,
358  ,      THIS PROC IS EXECUTED WHEN THE TERMINAL IS TAKEN OFF
358  ,      CHARGE WHILE IT IS TRYING TO CHARGE/DISCHARGE.
358  ,      AN ERROR MESSAGE IS DISPLAYED AND THE USER HAS 30 SECONDS
358  ,      TO PLACE THE UNIT BACK ON CHARGE UNTIL THE TEST IS ABORTED.
358  ;
358       KBD_SAVE = KBD_BUFFER                     ;SAVE DISPLAY
361       KK = 5                                    ;GIVE 30 SECONDS TILL ABORT
364       REPEAT
364         OUT(KBD)(KB_HOME)'CHARGER ',BEL
374         WAIT 60                                  ;GIVE TIME TO UPDATE DISPLAY
377         KK = KK - 1
382         GETCTL(URT) CURR_EIA, UR_SIGNALS
386       UNTIL ((KK = 0) OR (CURR_EIA AND UR_CHARGE))
395       IF KK = 0 THEN
399         PUTCTL(URT) SAVE_LOW, UR_SET,
399   &                  UR_DTR+UR_RTS+UR_RCT+UR_TXD+UR_SCAN+DISCHARGE+
399   &                  UR_BACKUP+CHARGE_CNTL, UR_RESET
408                                                 ;RESTORE ORIGINALS
408         PUTCTL(KBD) KB_UNLOCK
412         RESPONSE = INPUT(E,'TEST ABORTED.' & BEL)
423         RETURN MASTER_CONTROL
426       ENDIF
426       KBD_BUFFER = KBD_SAVE                     ;RESTORE BUFFER
429       PUT(KBD)                                  ;REDISPLAY
431    END;
432
432
432  END INIT;  END OF PROGRAM PSBAT1P

   0  ERROR DIAGNOSTICS IN PSBAT1P    ( 0 ERROR,  0 WARNING )
 432  BYTES OF MODULE CODE STORAGE,    147 BYTES OF DATA STORAGE
  18  LITERALS GENERATED IN MODULE,    203 BYTES OF DATA AND POINTERS
  25  VARIABLES ACCESSED IN MODULE,    125 BYTES OF FIELD DEFINITIONS
 805  TOTAL BYTES IN OBJECT FILE

2936  WORDS OF COMPILER SPACE USED, 20000 WORDS AVAILABLE FOR ALLOCATION
```

CL 4/C Description of Functions and Features of an Embodiment Such as Shown in FIGS. 12-14 14

P At the time of development of the circuit of FIG. 13, a preliminary summary of available functions and features of the system of FIGS. 12 and 13 was prepared. A copy of excerpts from an edited version of this summary, directed to the commercial Model 121 data terminal unit utilizing the circuit of FIG. 13, is found hereafter.

Preliminary Summary of Present Functions and Features of the 121, Semi-Intelligent Battery Controller

The 121 Battery Controller coupled with existing real time clock and NSC-800 CPU integrates a maximum number of features with minimum circuit duplication for an extremely versatile yet low cost solution.

The controller is designed to match the NICAD-Battery characteristics with the 121 requirements and is software and user adjustable to match the customers changing needs.

The most outstanding features of this 121 battery controller combination are as follows:

** Conditioning Charge

The periodic use of this feature virtually eliminates the memory effect of voltage depression and extends normal battery service life @ 1 year. This is accomplished by a controlled deep discharge of both the main batteries and backups. Followed by a normal recharge for 12 hours then automatically switch to stand by charge.

** Capacity Test

The capacity of main and backup batteries can be measured to precisely indicate battery condition and determine when a conditioning charge is necessary or when batteries should be replaced. This is done by a full recharge (12 hours) followed by a controlled timed constant current deep discharge at a C/5 rate, where the capacity is measured by the NSC-800 processor and is displayed as % of full capacity available, followed by a regular charge.

* Charge Efficiency Test

Can be used to find optimum charge rate, charge time, or an indicator of poor battery performance. This test is performed by deep discharging the batteries followed by a timed constant current charge and a timed constant discharge, then the CPU calculates charge efficiency. A normal recharge cycle follows.

P * Normal Recharge

P A complete recharge is accomplished in 12 hours. At a constant current rate at C/8.3, recharge is controlled by the CPU and initiated by plugging unit into charger.

P ** Over-Charge Protection

P This feature prevents over-charge if unit is continually plugged in and out from a charger such as in route accounting. In addition, when the unit is unplugged from a charger, the CPU will increment an elapsed time counter by a constant of two minutes for every minute off charge, until a maximum of 12 hours has been incremented, (six hours of real time). When returned to charger the CPU will decrement from the incremented amount to determine charge time. Maximum charge time of 12 hours is set whenever the unit has been turned off.

P * Fuel Gauge Feature

P From a full charge, (when the charge counter is at Ø), the 121 can calculate operating time remaining. This is done by incrementing a counter by a constant for operating time and a constant for standby time to find the amp-hour drained from a fully charged battery pack.

P * Variable Recharge Rate

P A wide range of charge rates and times are under CPU control. Fast charge models could be made available with a resistor charge and appropriate software.

P ** Standby Holding Charge

P This feature keeps the batteries at full charge ready for use by charging them at a C/100 rate. Control by the CPU.

P ** Charge Indicator

P A positive indication of unit being plugged into charge is displayed regardless of on/off switch. Controlled by CPU.

P * Remote control and diagnostics can be performed or telecom of battery parameters.

P Battery testing and conditioning can be performed without an on-site inspection.

P * Self Diagnostic Battery Testing Capability

P Production - During manufacturing, units can be programmed to cycle batteries several times and measure their capacity to identify defective units before they leave the plant.

Field Test - Battery condition can be easily checked by Field Service.

User Test - The customer can check the condition of his batteries.

** Temperature Protection Over-Under

Over and under temperature protection is an integral part of the battery pack reducing possible abuse and promoting longer battery life. Units will taper back charge rate at low temperature below 10°C and cut back to trickle rates at high battery temperature above 55°C.

** Low Battery Indicator

Tells user when batteries must be recharged to prevent loss of memory data, giving the user a minimum of 30 minutes standby operation until recharge.

** Deep Discharge Indicator

During a discharge the controller tells CPU when batteries are completely discharged.

* All functions and features excluding (internal) temperature protection are under software control and thus can be modified for optimum performance throughout life.

** Battery pack hardware can accommodate 1/2D cells with only resistor changes from the 3/5C pack.

** The software and functions are the same with 1/2D or 3/5C cells so as to allow the changing of different packs if desired at a later date without changes internal to the 121 hardware or software.

** The present 121 design with the semi-intelligent battery controller remains hardware compatible with the "smart" battery pack.

Beyond this, the complete cost of all parts of the customer replaceable 121 semi-intelligent battery controller is less than $27 including four 3/5C cells. This is based on 100p quantities. Production quantities would represent a parts cost reduction.

* May be included for further reliability and functionality.

** Required features for reliable operation in all applications.

Definition of 121 Battery Pack Control Lines

- Charge Control (P 3-5)

  $\overline{\text{CHARGE CONTROL}}$, Standby charge
  Rate c/100

  CHARGE CONTROL, Full charge
  Rate C/8.3

- Discharge (P 3-4)

  $\overline{\text{DISCHARGE}}$, Discharge is disabled
  LB1 is activated

  DISCHARGE, Discharge is enabled
  at a -c/5 rate
  LB2 is now active

- LB1/LB2 (P 3-1)

  LB1 is the low battery detect of 4.65 volts and is reset high at 5.4V.

  $\overline{\text{LB1}}$, indicates low battery
  LB1, not low battery

  LB2 is the discharged detect of 3.8 volts and is reset high at 5.4V.

  $\overline{\text{LB2}}$, indicates main and backups are completly discharged
  LB2, not discharged

- +BATT (P 3-2)

  Normally +5 volts from 4 cell battery

- -BATT (P 3-6)

  Ground line

- CHARGE

  Is a constant current charge limited to .66 amp on the CPU board.

CL4 121 Semi-Intelligent Battery Controller

Operational Sequence of Required Features

P — CHARGE COUNTER

Is a software function to simplfy battery pack operational description.

P1 1) Charge counter enables the charge control

- Charge counter >0, charge control high
- Charge counter =0, charge control low

P1 2) Counter is decremented by real time to zero when charge control is high.

P1 3) Counter is incremented by two times real time up to a maximum of 12 hours whenever unit is taken off charge while turned on.

4) If the unit is turned off and not plugged in to charge, then on power up, counter will set to 12 hours.

5) Counter is set to 12 hours when LB1 or LB2 is present.

6) Discharge sets counter to zero.

P — NORMAL RECHARGE/OVER CHARGE PROTECTED

P1 1) When unit is plugged into charger and charge counter is zero.

P1 2) Charge control will always be low if not plugged in to charge.

P — STAND-BY CHARGE

1) When unit is plugged into charger and charge counter is zero.

P — LOW BATT (DISPLAY)

1) Will be displayed during $\overline{LB1}$ or $\overline{LB2}$

P — BATT RECHARGING (DISPLAY)

P1 1) When plugged into charge it will always be enabled in one of two modes.

P2 A) Will be on steady when charge counter is zero, signifying a full charge or that a user selectable function is complete.

P2 (B) Will blink on and off when charge counter is not zero or user selectable function is in progress.

P 9 CHARGING FUNCTION AND STATUS (DISPLAY)

When unit is turned off or on and plugged into charger if possible

P1 1) Indicate if a user selectable function is in progress and the time remaining to end of function.

P1 2) During normal recharge display the charge counter time such as

TIME TO FULL RECHARGE XX:XX and FULL RECHARGE READY

P *9 CONDITIONING CHARGE

P1 1) Key in "CONDITIONING CHARGE"

2) Discharge until $\overline{LB2}$

3) Display "CONDITIONING COMPLETE"

*9 CAPACITY TEST

1) Key in "CAPACITY TEST"

2) Charge until charge counter is zero

3) Discharge until $\overline{LB2}$

4) Discharge time/s is the percent of full rated capacity

5) Display "XXX % CAPACITY AVAILABLE"

+LG *USER SELECTABLE BATTERY FUNCTIONS

These functions can only be started and performed while charger is plugged in with unit turned on. If charger is unplugged before function is complete, then cancel and display "TEST INVALID".

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CL 1/2 Description of an Embodiment
Corresponding to FIGS. 12-14
for Conditioning Spare Battery Packs

P As previously explained the embodiment of FIGS. 12, 13 and 14 can represent a stationary battery conditioning system, for example for conditioning nickel cadmium battery packs of the Model 121 portable data terminal unit as described herein.

13 The following shows a copy of a preliminary summary of recommendations for a charger system to be used with spare battery packs for the Model 121.

The "smart" battery pack is shown by FIGS. 2, 3, 4, 5, 9A, 9B, 10 and 11 herein.

P This report contains a preliminary summary of recommendations for a dual charger system to be used with spare NT121 battery packs.

P Its intended use is to charge spare NT121 battery packs consistent with all functions and features of the NT121 controller combination to ensure equivalent life and reliability is achieved.

The applicable functions of the 121 battery charger are as follows:

P
- Conditioning Charge
- Capacity Test
- Normal recharge
- Over-charge Protection
- Variable Recharge Rate
- Standby Charge
- Charge Indicator
- Low Battery Indicator
- Deep Discharge Indicator
- Software Control
- Hardware Control
- Hardware Compatible with Smart Battery Pack

Conditioning Charge

The periodic use of this feature virtually eliminates the memory effect of voltage depression and extends normal battery service life to one year. This is accomplished by a controlled deep discharge of both the main batteries and backups. This is followed by a normal recharge for 12 hours, then automatically switched to standby charge.

Capacity Test

The capacity of the battery pack can be measured precisely to indicate battery condition and can determine when batteries shoucl be replaced. This is done by a full recharge (12 hours) followed by a constant current deep discharge at a C/8 rate where the capacity is measured and displayed as percent of full capacity or absolute capacity in amp hours. This is followed by a regular charge.

Normal Recharge

A complete recharge is accomplished in 12 hours at a constant current rate of C/8.3. Recharge is controlled by the CPU and initiated by the charge counter or the user.

Over-Charge Protection

This feature prevents over-charge and keeps the battery at a full charge. When the unit is unplugged from a power source, the CPU will increment an elapsed time counter by a constant of one minute for every 20 minutes off charge. Until a maximum of 12 hours has been reached (10 days of real time) when returned to a charge, the CPU will decrement from the incremented time to determine charge time. Maximum charge time of 12 hours is set whenever the batteries are removed from the holder.

Variable Recharge Rate

A wide range of charge rates and times are under CPU control. Fast charge models could be made available with a resistor charge and appropriate software.

Stand-by Holding Charge

This feature keeps the batteries at full charge ready for use by charging them at a C/100 rate. Control by the CPU.

Charge Indicator

A positive indication of unit being plugged into charge is displayed regardless of on/off switch. Controlled by CPU.

Full Charge Indication

To indicate to the user that the battery pack is fully charged and ready for use.

Low Battery Indicator

Indicates a dead battery. May not be required.

Deep Discharge Indication

Indicates a deep discharge is complete. May not be required.

Software Control

For ease of future modification if required.

Hardware Compatible with the "smart" battery pack.

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It will be apparent that many modifications and variations may be made without departing from the scope of the teachings and concepts of the present invention.

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